FIG. 1

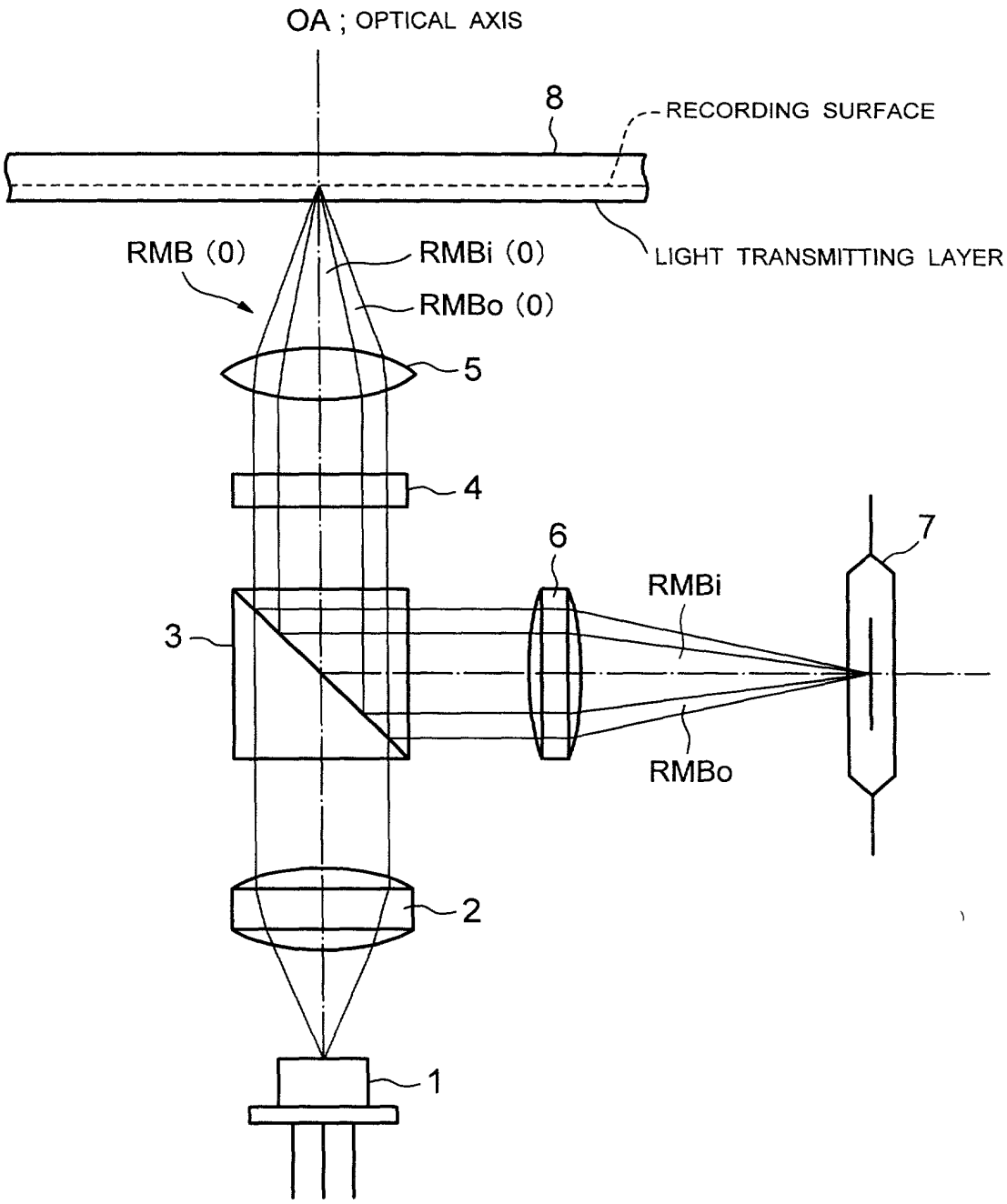

OA ; OPTICAL AXIS
8
RECORDING SURFACE
LIGHT TRANSMITTING LAYER
RMB (0)
RMBi (0)
RMBo (0)
5
4
6
7
RMBi
3
RMBo
2
1

FIG. 2

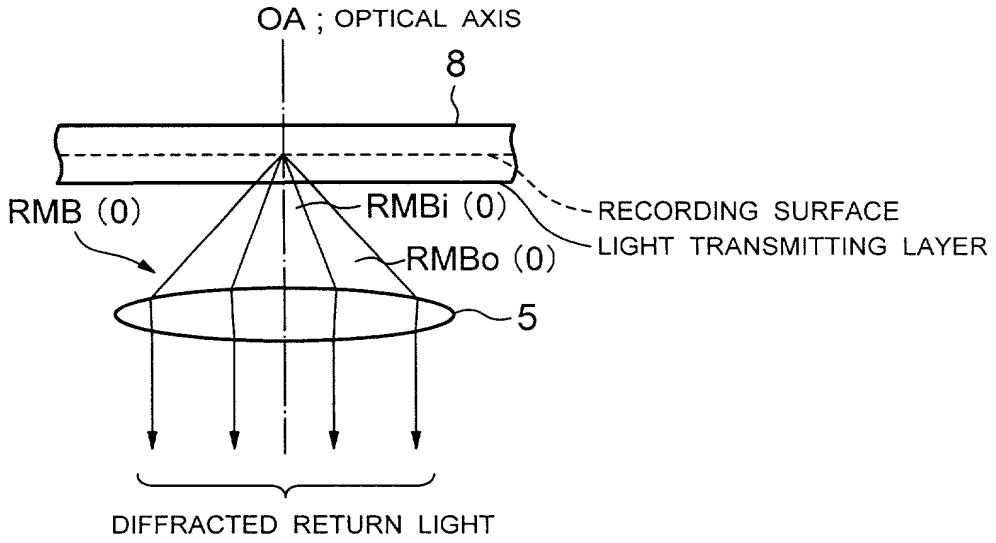

OA ; OPTICAL AXIS
8
RMB (0)
RMBi (0)
RMBo (0)
RECORDING SURFACE
LIGHT TRANSMITTING LAYER
5
DIFFRACTED RETURN LIGHT

FIG. 3

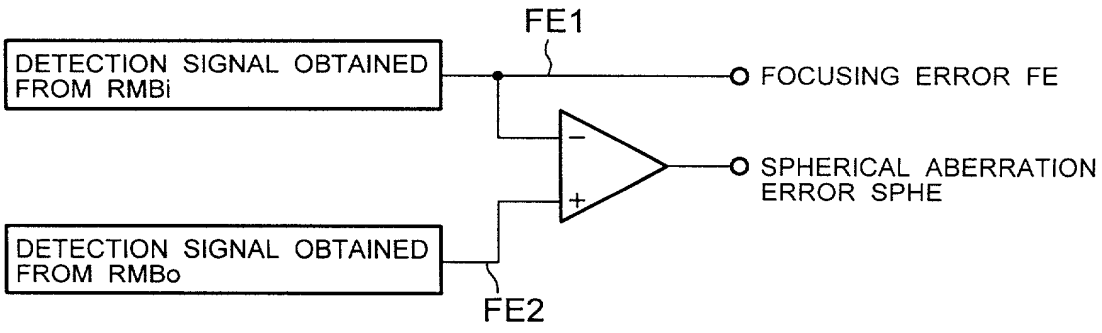
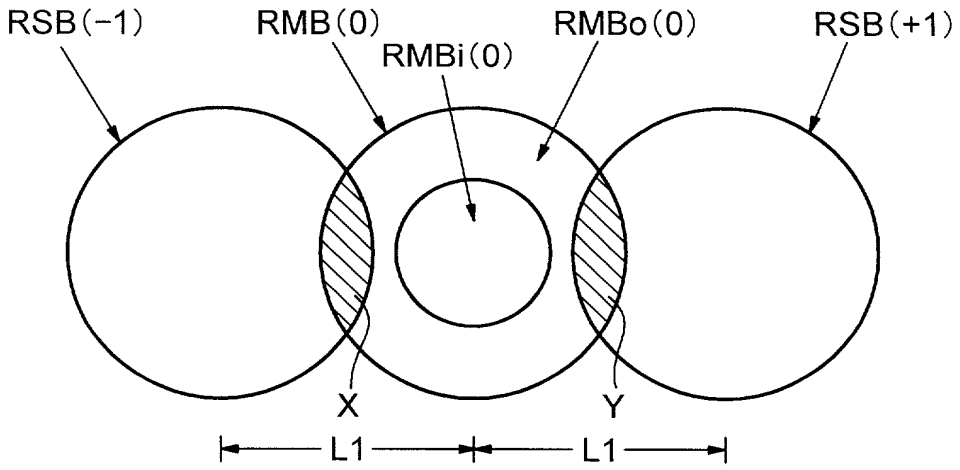
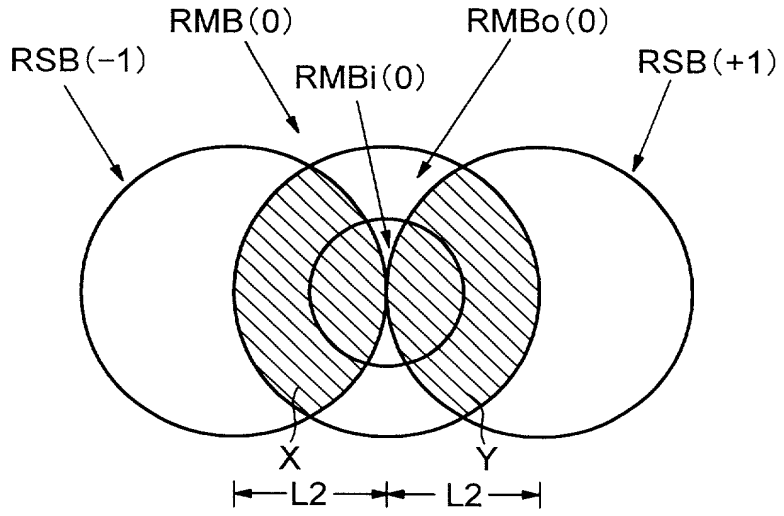

FE1
DETECTION SIGNAL OBTAINED FROM RMBi
FOCUSING ERROR FE
SPHERICAL ABERRATION ERROR SPHE
DETECTION SIGNAL OBTAINED FROM RMBo
FE2

FIG. 4



POSITIONAL RELATION BETWEEN THE 0-TH ORDER LIGHT AND THE ±1 PRIMARY DIFFRACTED LIGHT WHEN THE NUMERICAL APERTURE NA IS SMALL IN THE IN-FOCUS STATE OR WHEN THE TRACK PITCH TP IS SMALL IN THE IN-FOCUS STATE.
RMB(0):0-TH ORDER LIGHT, RMBi(0):INNER RADIUS LIGHT, RMBo(0):OUTER RADIUS LIGHT, RSB(−1):−1 PRIMARY DIFFRACTED LIGHT, RSB(+1):+1 PRIMARY DIFFRACTED LIGHT

FIG. 5

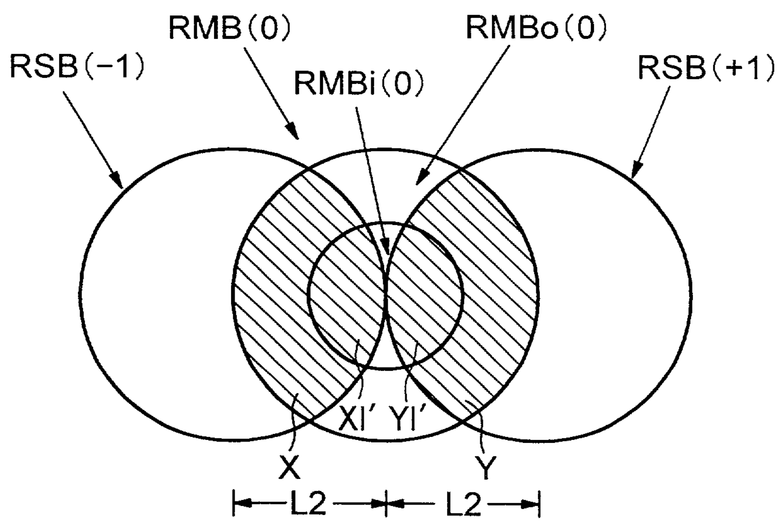


POSITIONAL RELATION BETWEEN THE 0-TH ORDER LIGHT AND THE ±1 PRIMARY DIFFRACTED LIGHT IN A CASE WHERE THE NUMERICAL APERTURE NA IS LARGE IN THE IN-FOCUS STATE OR IN A CASE WHERE THE TRACK PITCH TP IS LARGE IN THE IN-FOCUS STATE.

JP2004-095096 A 2004.03.25

09756306.012401

FIG. 6



(POSITIONAL RELATION BETWEEN THE 0-TH ORDER LIGHT AND THE ±1 PRIMARY DIFFRACTED LIGHT WHEN THE NUMERICAL APERTURE NA IS LARGE AND IN THE DEFOCUSING STATE, OR WHEN THE TRACK PITCH TP IS LARGE AND IN THE DEFOCUSING STATE.)

FIG. 7

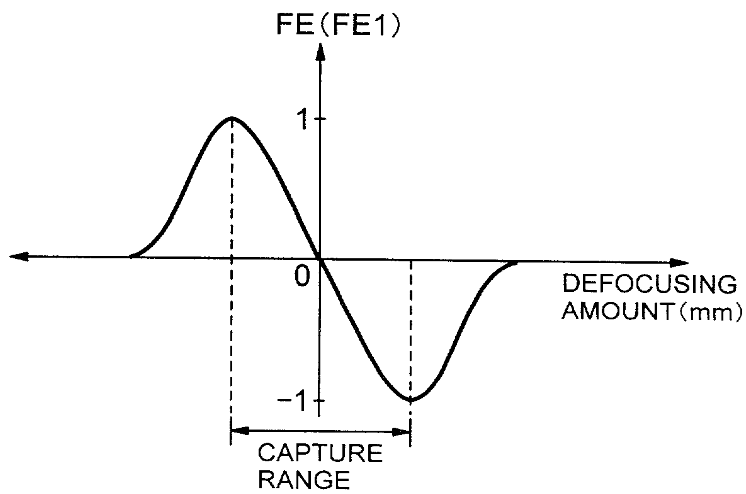

FE(FE1)
1
0
-1
DEFOCUSING
AMOUNT(mm)
CAPTURE
RANGE

FIG. 8

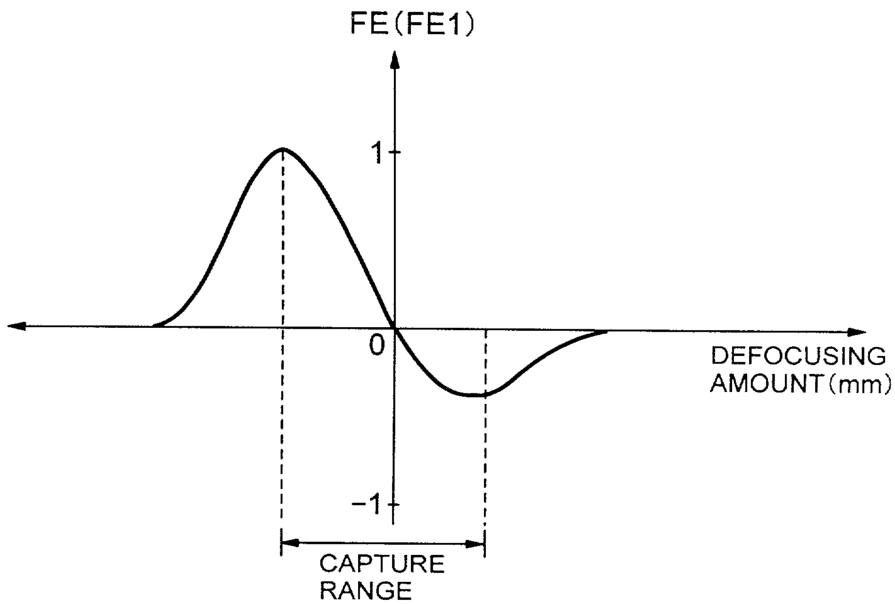

FE(FE1)
1
0
-1
DEFOCUSING
AMOUNT(mm)
CAPTURE
RANGE

FIG. 9

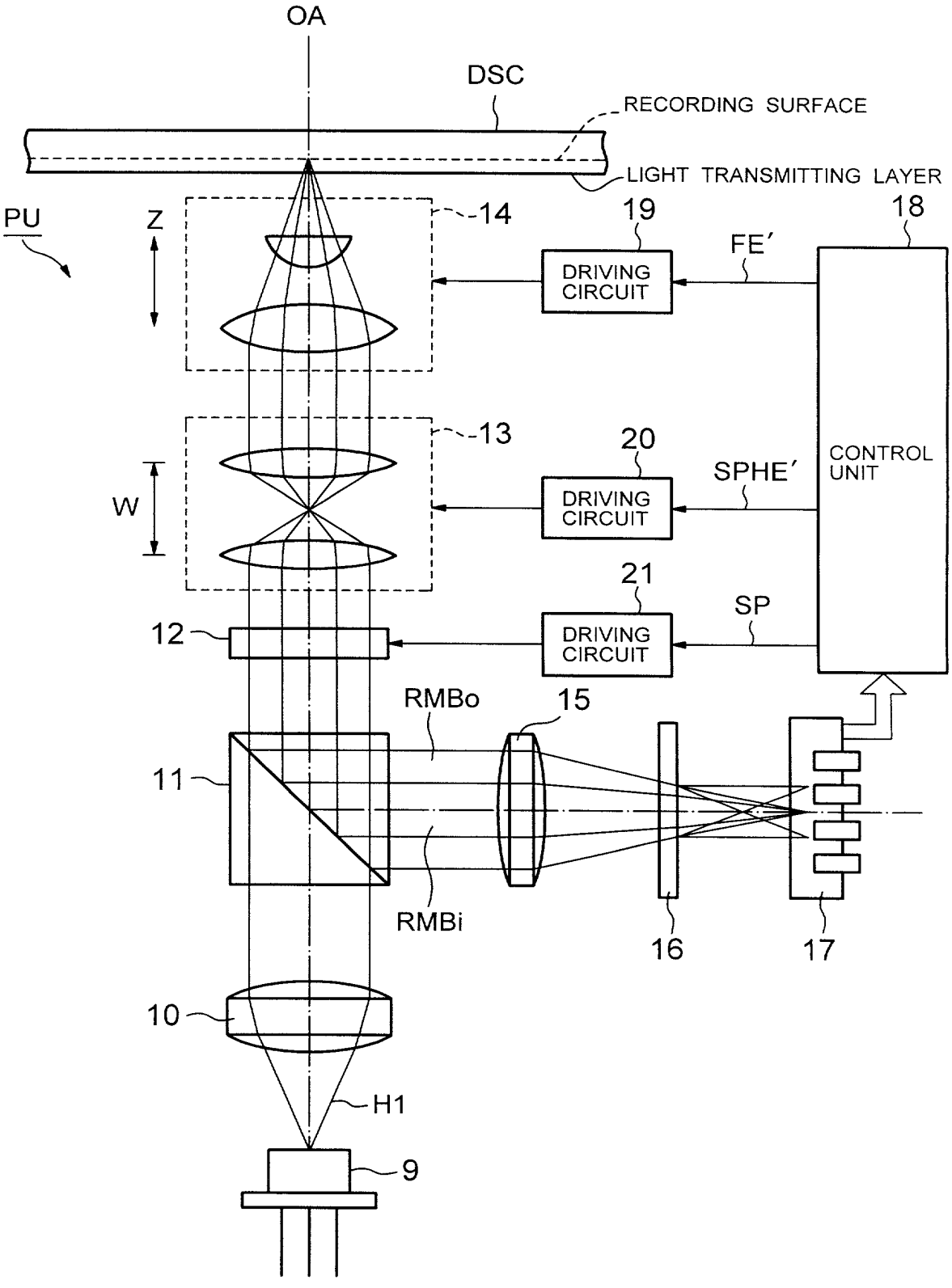

OA
DSC
RECORDING SURFACE
LIGHT TRANSMITTING LAYER
PU
Z
14
19
18
FE'
DRIVING CIRCUIT
13
20
SPHE'
CONTROL UNIT
W
DRIVING CIRCUIT
21
SP
12
DRIVING CIRCUIT
RMBo
15
11
RMBi
16
17
10
H1
9

FIG. 10

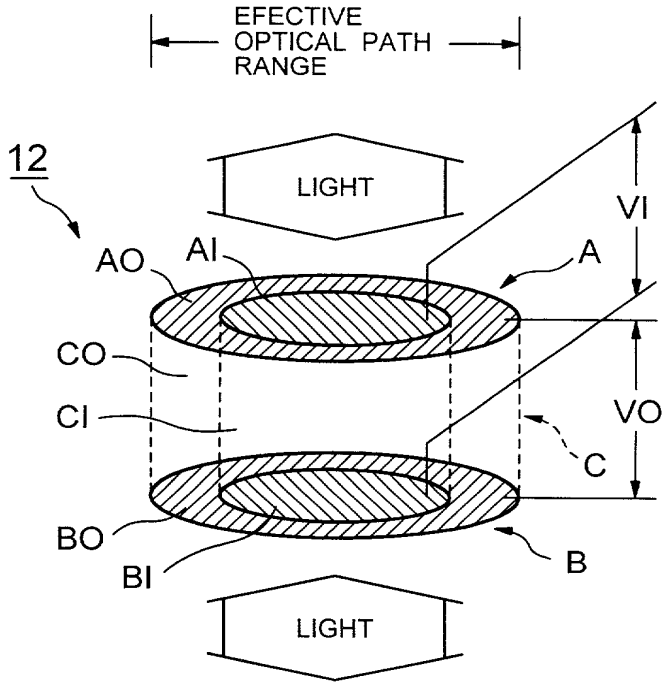
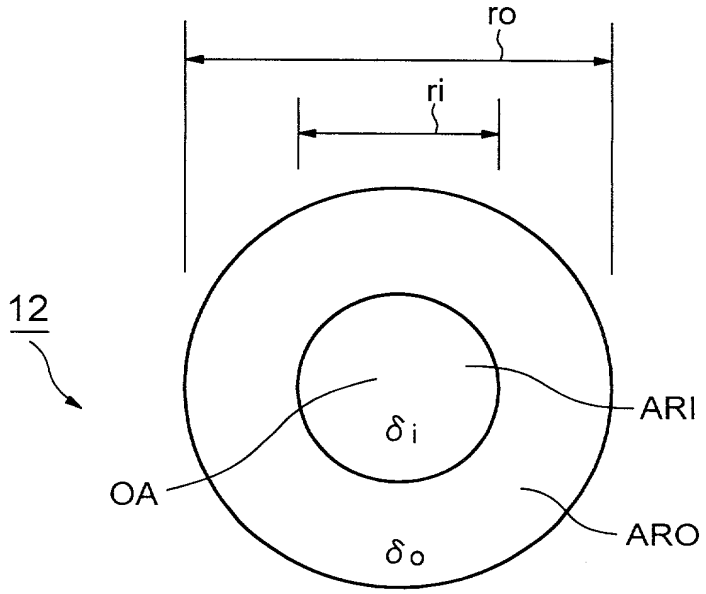


FIG. 11



09765206-042304

FIG. 12

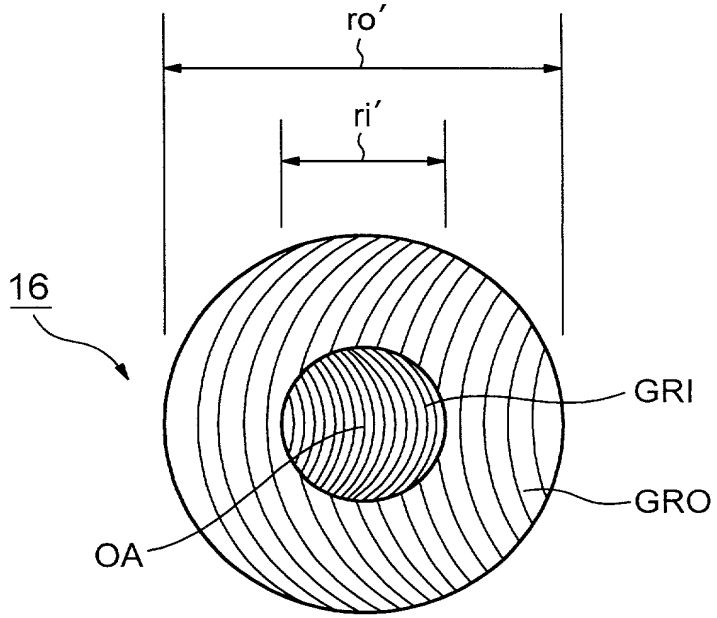

ro′
ri′
16
GRI
GRO
OA

FIG. 13

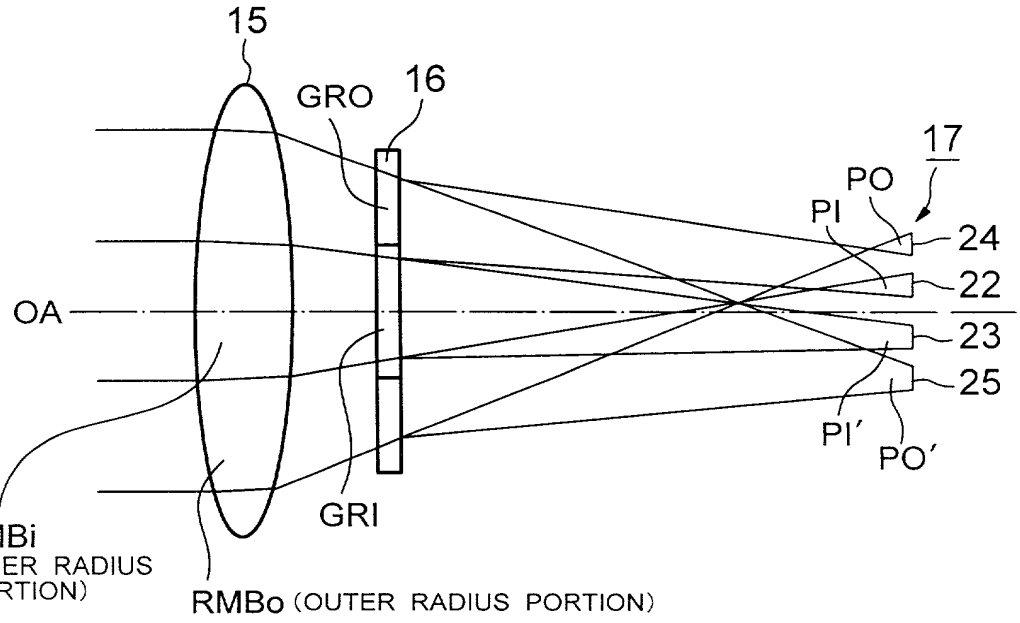

15
GRO
16
17
PO
PI
24
22
OA
23
25
PI′
PO′
GRI
RMBi
(INNER RADIUS PORTION)
RMBo (OUTER RADIUS PORTION)

FIG. 14

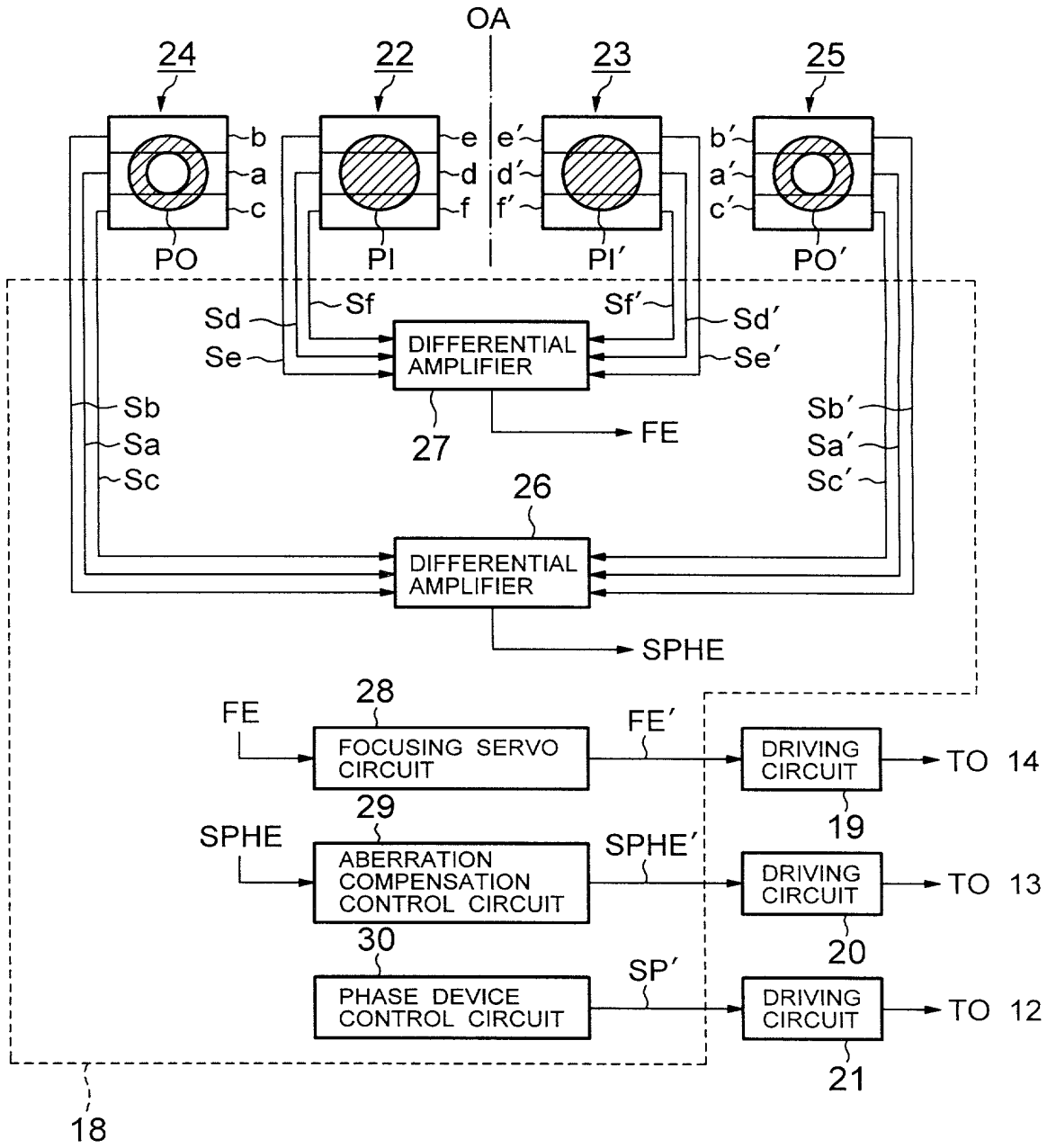
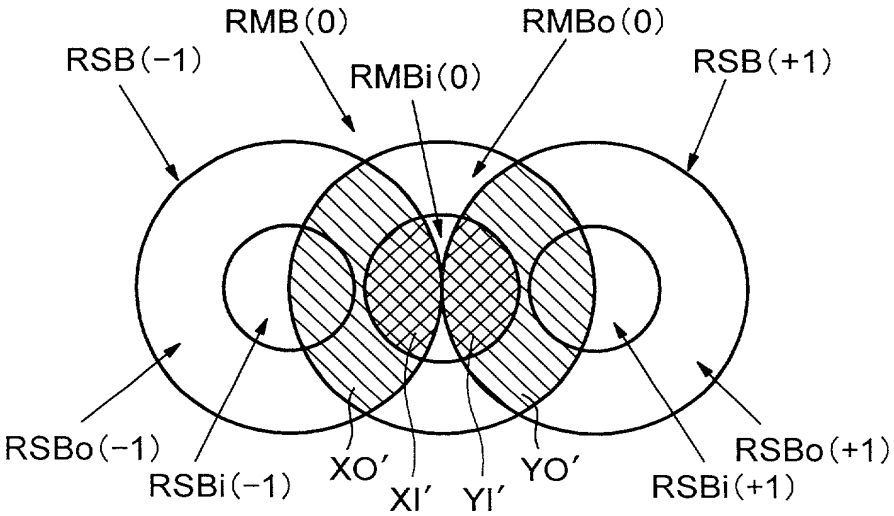

OA
24
22
23
25
b
a
c
e
d
f
e′
d′
f′
b′
a′
c′
PO
PI
PI′
PO′
Sd
Se
Sf
Sf′
Sd′
Se′
DIFFERENTIAL AMPLIFIER
27
FE
Sb
Sa
Sc
Sb′
Sa′
Sc′
26
DIFFERENTIAL AMPLIFIER
SPHE
FE
28
FOCUSING SERVO CIRCUIT
FE′
DRIVING CIRCUIT
TO 14
19
SPHE
29
ABERRATION COMPENSATION CONTROL CIRCUIT
SPHE′
DRIVING CIRCUIT
TO 13
20
30
PHASE DEVICE CONTROL CIRCUIT
SP′
DRIVING CIRCUIT
TO 12
21
18

FIG. 15



JP2014-095950A 2014.05.22

FIG. 16

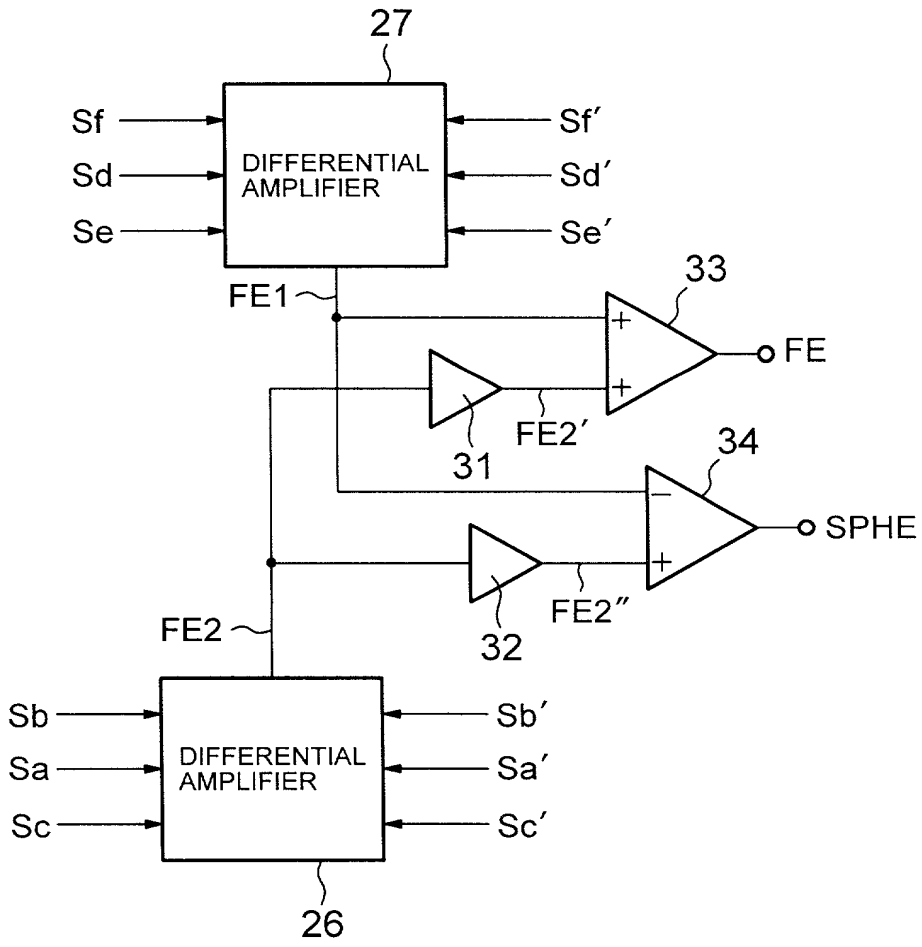

27
Sf
Sd
Se
DIFFERENTIAL AMPLIFIER
Sf′
Sd′
Se′
FE1
33
FE
FE2′
31
34
SPHE
FE2″
32
FE2
Sb
Sa
Sc
DIFFERENTIAL AMPLIFIER
Sb′
Sa′
Sc′
26

FIG. 17

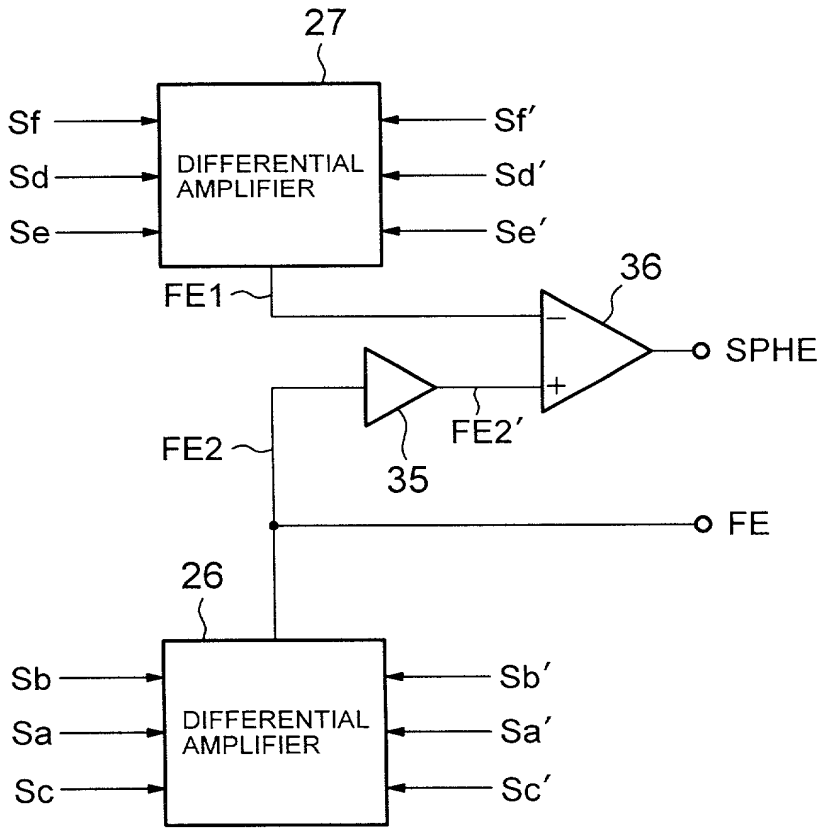

27
Sf
Sd
Se
DIFFERENTIAL AMPLIFIER
Sf′
Sd′
Se′
36
FE1
SPHE
FE2′
FE2
35
FE
26
Sb
Sa
Sc
DIFFERENTIAL AMPLIFIER
Sb′
Sa′
Sc′

FIG. 18

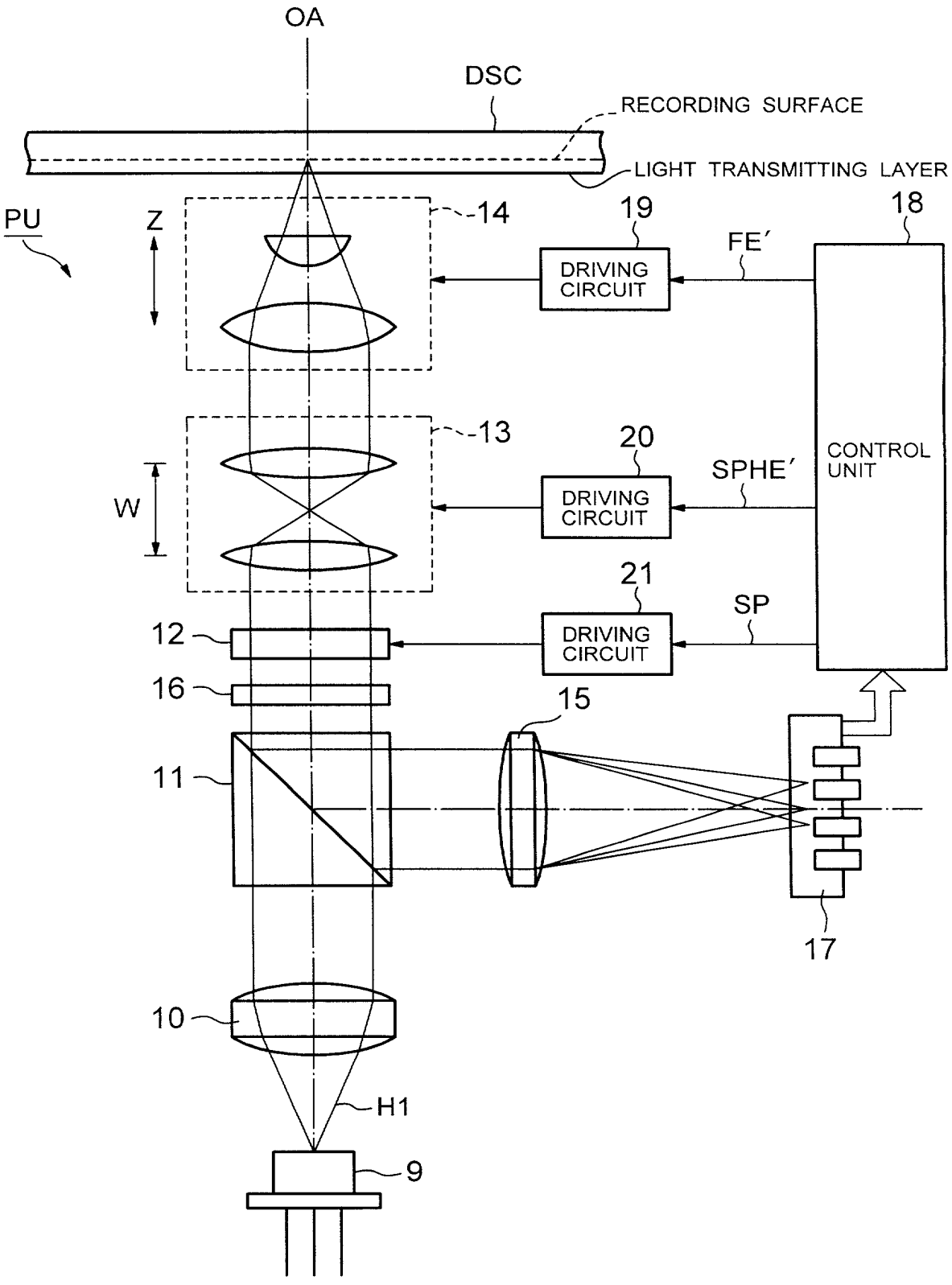

OA
DSC
RECORDING SURFACE
LIGHT TRANSMITTING LAYER
PU
Z
W
14
13
12
16
11
10
H1
9
15
17
18
19
20
21
FE′
SPHE′
SP
DRIVING CIRCUIT
DRIVING CIRCUIT
DRIVING CIRCUIT
CONTROL UNIT

FIG. 19

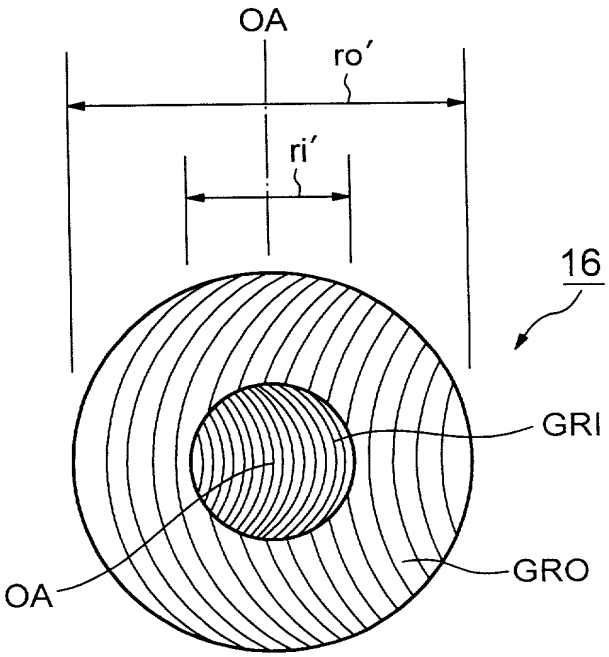


FIG. 20